PI3EQXDP1201
Demo Board Rev.A User Manual

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1 Introduction

PI3EQXDP1201 DisplayPort 1.2 re-driver is designed for source application. PI3EQXDP1201 is DisplayPort 1.1a and 1.2 standard compliant. It supports dual-mode displayPort inputs as well as outputs. This user manual describes the components and the usage of PI3EQXDP1201 demo board rev.A.

2 Overview

Figure 1 is the block diagram of Pericom PI3EQXDP1201 demo board rev.A and figures 2 and 3 show the top and bottom views of the demo board rev.A. One DP plug connector (J1) on PI3EQXDP1201 demo board rev.A is used for plugging a source device, such as a motherboard. A DP cable can be connected between a DP receptacle connector (J2) on the demo board rev.A and a sink device, such as a DP monitor. VDD_3.3V for the entire demo board rev.A is supplied from the DP source through pin 20 of the DP plug connector. VDD_1.5V will be provided through a regulator (U2) for PI3EQXDP1201 on the demo board rev.A if dual power supply is chosen. Swing, pre-emphasis and equalization can be controlled via pins or SMBus. External pull-ups on SCL_CTL and SDA_CTL pins of PI3EQXDP1201 are required before enabling SMBus for EQ setting.

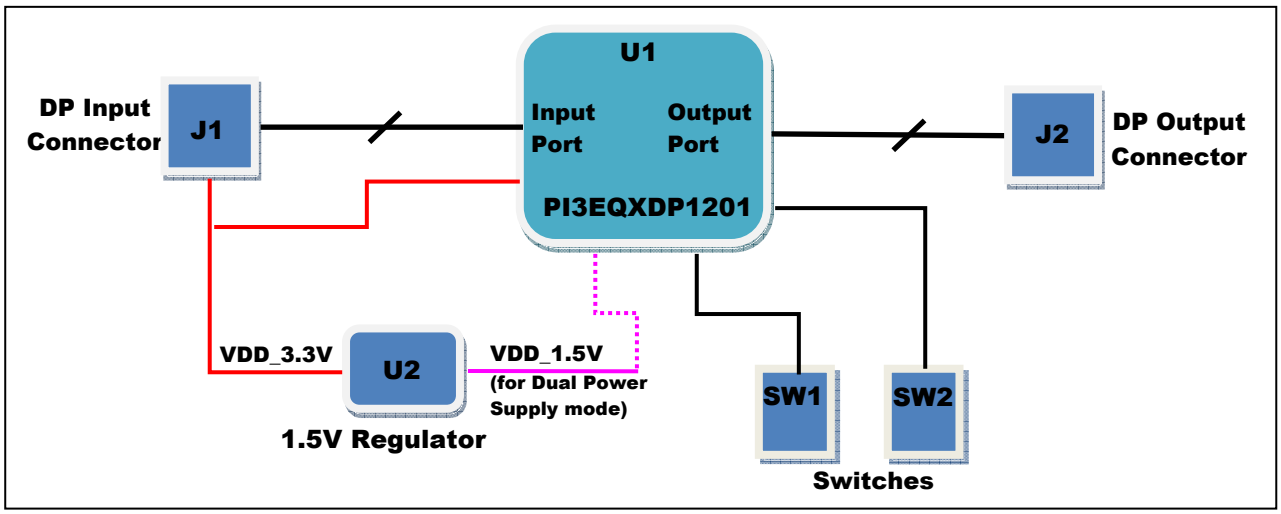


Figure 1: Block Diagram of PI3EQXDP1201 Demo Board Rev.A

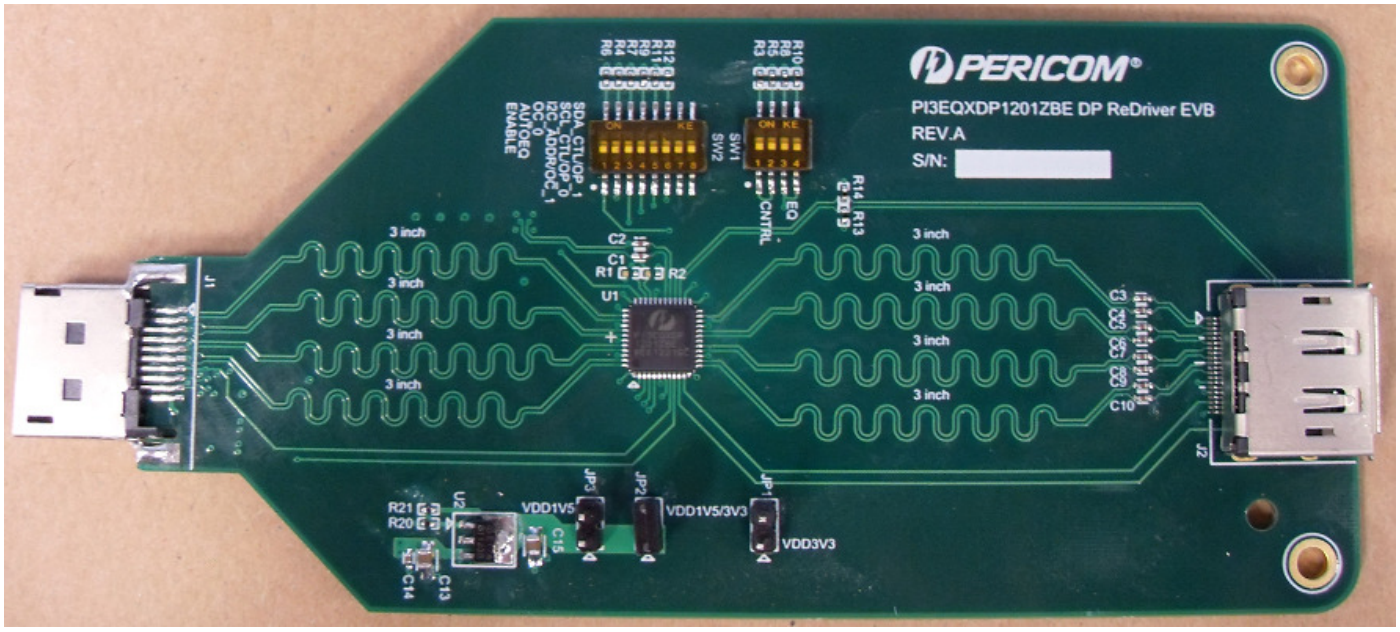


Figure 2: Top View of PI3EQXDP1201 Demo Board Rev.A

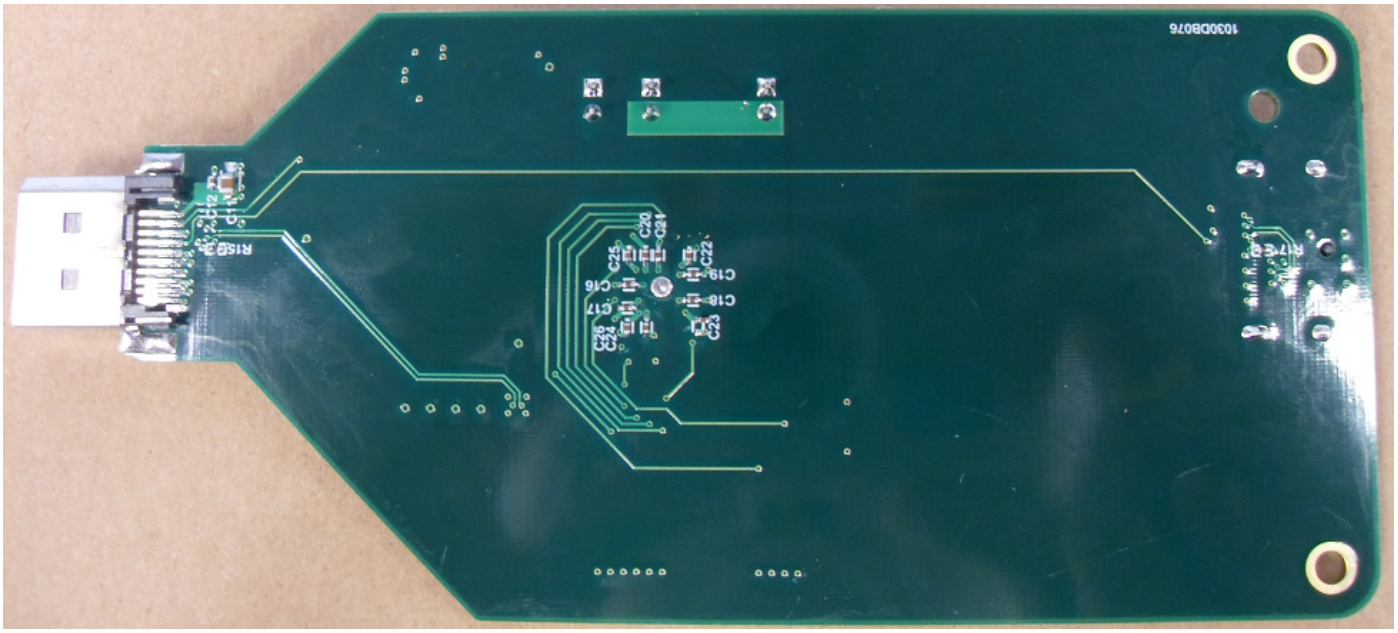


Figure 3: Bottom View of PI3EQXDP1201 Demo Board Rev.A

3 Quick Start

To start-up the PI3EQXDP1201 demo board rev.A, complete the following steps:

1. Short header pin JP2 to set PI3EQXDP1201 to single power supply condition;
2. Open all the switches on SW1 and SW2 to enable Auto Eq mode 2 and to follow DPCD register settings;
3. Connect a source device, e.g. a motherboard, to DP input connectors at J1;
4. Connect a sink device, e.g. DP monitor, to DP output connector at J2.

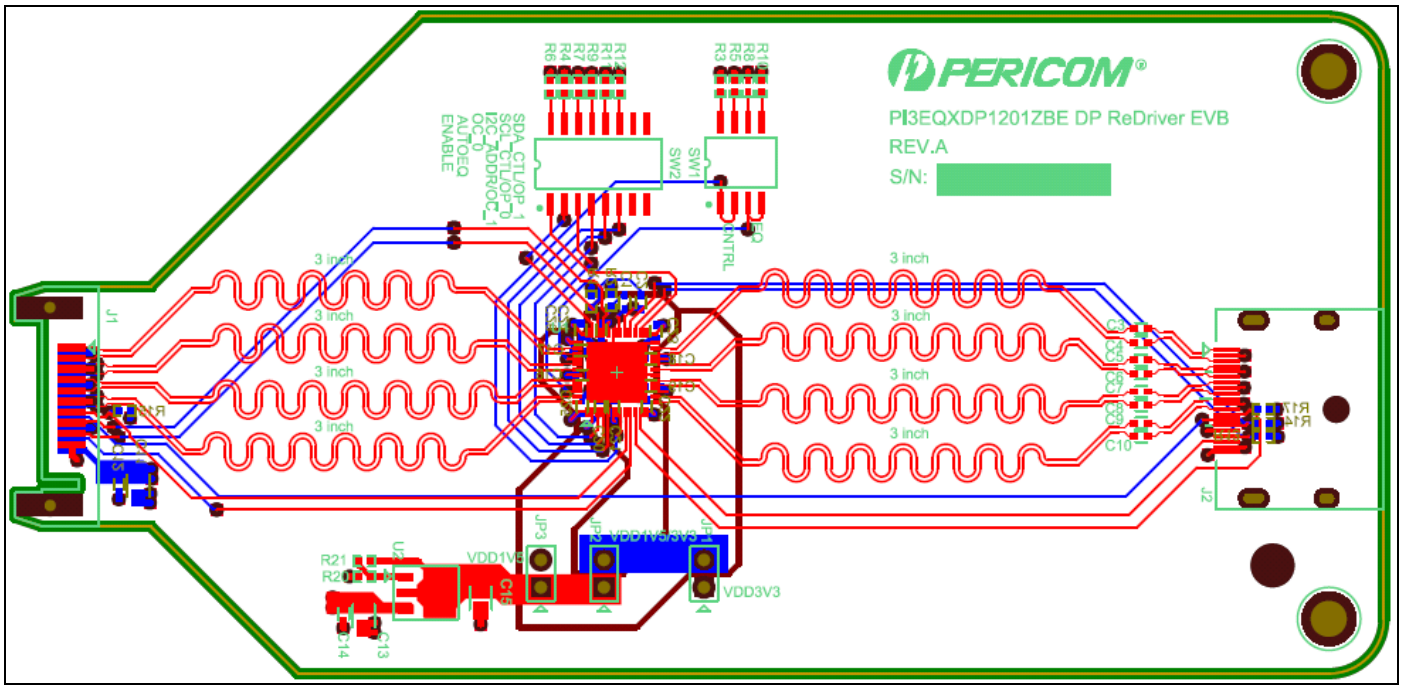


Figure 4: Layout of PI3EQXDP1201 Demo Board Rev.A

4 Circuit Description

4.1 Single or Dual Power Supply Option

PI3EQXDP1201 offers two configurations of power supply mode. For convenience, 3.3V single power supply can be selected. For power saving, 3.3/1.5V dual power supply mode is more preferable. On PI3EQXDP1201 demo board rev.A, header pins are used to select connecting 3.3V or 1.5V power plane to VCORE pins. To select 3.3V single power supply, short pins 1 and 2 of header JP1 on the demo board rev.A. Conversely, to select dual 3.3/1.5V power supply mode, short pins 1 and 2 of both headers JP2 and JP3.

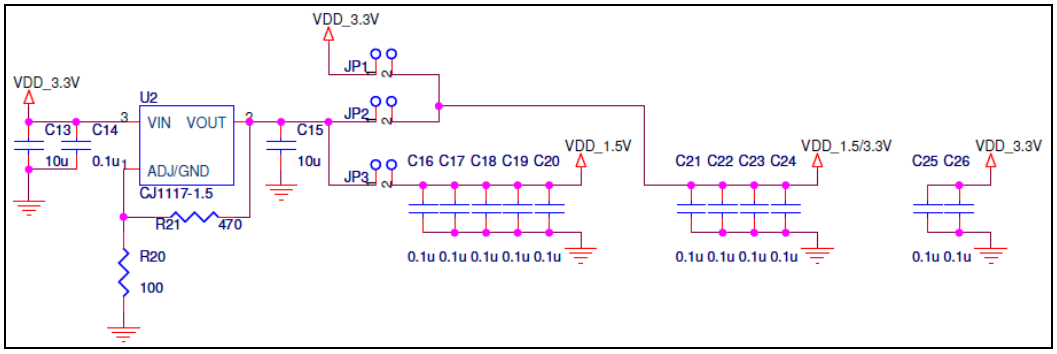


Figure 5: Single/Dual Power Supply Configuration of PIEQXDP1201 Demo Board Rev.A

4.2 Control Pin Settings

Two switches on demo board rev.A, namely SW1 and SW2, are used to set CNTRL, EQ, ENABLE, Auto-EQ, OC_0, I2CD_ADDR/OC_1, SCL_CTL/OP_0 and SDA_CTL/OP_1 control pins. As all the pins have internal pull-up resistors, external pull-down resistors are designed on the demo board rev.A.

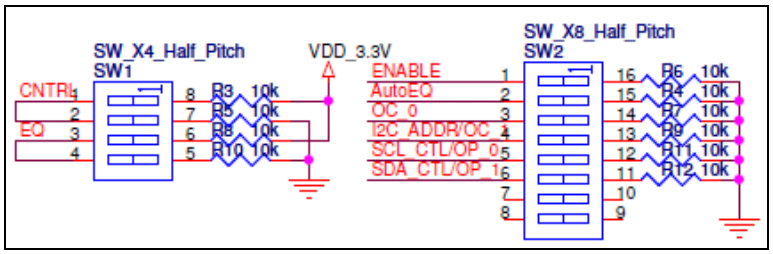


Figure 6: Control Pin Settings of PIEQXDP1201 Demo Board Rev.A

4.3 External SCL_CTL and SDA_CTL Pull-ups

When SMBus register is enabled, pins 4 and 5 of PI3EQXDP1201 are used as SCL_CTL and SDA_CTL for SMBus transaction. As internal pull-up resistors of these two pins are weak, stronger external pull-ups should be added for SMBus controller to read/write PI3EQXDP1201 properly.

5 Equalization, Swing and Pre-emphasis Settings

Equalization, swing and pre-emphasis of PI3EQXDP1201 can be controlled via pins or SMBus.

5.1 Equalization Setting via Pin Control

PI3EQXDP1201 offers flexible equalization setting. Three Auto Eq Modes and three Fixed Eq Modes can be selected.

EQ (Pin 40)	Auto-EQ (Pin 35)	Equalization Function	Pre-emphasis Set (DPCD 00103-6h)	EQ Value		
				1.62G	2.7G	5.4G
L	H	Auto Eq Mode 1	0 0	2.26	2.74	2.49
			0 1	0.34	0.57	0.22
			1 0	-1.42	-2.01	-2.79
			1 1	-2.39	-3.62	4.71
M	H	Auto Eq Mode 2	0 0	3.97	5.92	7.30
			0 1	1.44	2.50	3.41
			1 0	0.34	0.57	0.22
			1 1	-1.42	-2.01	-2.79
H	H	Auto Eq Mode 3	0 0	3.97	7.27	8.69
			0 1	3.21	5.10	6.42
			1 0	1.44	2.50	3.41
			1 1	0.34	0.57	0.22
L	L	Fixed Eq; 2.5dB@2.7GHz	X X	1.44	2.50	3.41
M	L	Fixed Eq; 5.1dB@2.7GHz	X X	3.21	5.10	6.20
H	L	Fixed Eq; 7.2dB@2.7GHz	X X	3.97	7.27	8.69

Table 1: EQ Setting of PI3EQXDP1201 Demo Board Rev.A

5.2 Swing and Pre-emphasis Settings via Pin Control

Swing and pre-emphasis settings of PI3EQXDP1201 are designated to use DPCD register setting or to override the register setting.

CNTRL (Pin 7)	CAD_SNK (Pin 10)	OC_[1:0] (Pins 3,46)	OP_[1:0] (Pins 5,4)	SMBus Byte1 bit1	Output Swing	Pre-emphasis	Aux Listener
M	0	1 X	X X	X	Register setting	Follow listener	ON, use DPCD register setting
M	0	0 0	X X	X	800 mV	0 dB	ON, override register setting
M	0	0 1	X X	X	600 mV	3.5 dB	ON, override register setting
M	1	X X	X X	X	800 mV	0 dB	OFF, override register setting
L	0	X X	X X	X	Follow listener	Follow listener	ON, use SMBus register setting
L	1	X X	X X	X	800 mV	0 dB	OFF, override register setting
H	X	0 0	0 0	0	400 mV	0 dB	OFF, override register setting
H	X	0 1	0 1	0	600 mV	3.5 dB	OFF, override register setting
H	X	1 0	1 0	0	1200 mV	9 dB	OFF, override register setting
H	X	1 1	1 1	0	800 mV	0 dB	OFF, override register setting

Note: “M” means V3p3/2 voltage level.

Table 2: OC and OP Settings of PI3EQXDP1201 Demo Board Rev.A

5.3 Equalization Setting via SMBus Control

On top of pin control, SMBus can be used to set link bandwidth, lane count, equalization, swing and pre-emphasis, etc, of PI3EQXDP1201. Upon using SMBus, user must set byte17 bit1 of SMBus register to 1. I2C_ADDR pin 3 of PI3EQXDP1201 is used to select particular I2C address, i.e. 0xA8 if I2C_ADDR is set to low or 0xAA if I2C_ADDR is set to high.

SMBus Address	R/W	Data Bytes
A8 or AA	W	11, 00, 01

Table 3: Enabling SMBus of PI3EQXDP1201 Demo Board Rev.A

The three data bytes above represent:

1. 11h represents SMBus register byte 17 in hex;
2. 00h is the offset;
3. 01h sets Byte17 bit1 to 1 to enable SMBus mode.

After enabling SMBus mode, equalization setting of PI3EQXDP1201 can be selected through SMBus register Byte 0 bit[3:0].

SMBus Byte 0 bit[7:4]	EQ Value		
	1.62G	2.7G	5.4G
0000	0.47 dB	0.89 dB	1.49 dB
0001	-2.39 dB	-3.62 dB	-4.71 dB
0010	0.78 dB	1.34 dB	1.95 dB
0011	-2.08 dB	-3.17 dB	-4.25 dB
0100	1.44 dB	2.50 dB	3.41 dB
0101	-1.42 dB	-2.01 dB	-2.79 dB
0110	2.41 dB	3.90 dB	5.16 dB
0111	-0.45 dB	-0.58 dB	-1.03 dB
1000	3.21 dB	5.10 dB	6.42 dB
1001	0.34 dB	0.57 dB	0.22 dB
1010	3.97 dB	5.92 dB	7.30 dB
1011	1.10 dB	1.39 dB	1.09 dB
1100	4.55 dB	7.27 dB	8.69 dB
1101	2.26 dB	2.74 dB	2.49 dB
1110	6.96 dB	9.28 dB	10.8 dB
1111	4.00 dB	4.76 dB	4.64 dB

Table 4: SMBus EQ Setting of PI3EQXDP1201 Demo Board Rev.A

If setting the equalization value to the highlighted set above, 76h will be written to byte 0 where bit[3:0] are reserved and the default value of 0110 cannot be changed.

SMBus Address	R/W	Data Bytes
A8 or AA	W	00, 00, 76

Table 5: Equalization Setting of PI3EQXDP1201 via SMBus

5.4 Swing and Pre-emphasis Settings via SMBus Control

After enabling SMBus control as mentioned in the previous section, swing and pre-emphasis settings of PI3EQXDP1201 can also be selected through SMBus register Bytes 4-7, which are the same as DPCD registers 00103-6h. Bytes 4, 5, 6 and 7 are the registers for lane settings for lanes 0, 1, 2 and 3, respectively.

SMBus Byte 4-7 bit[1:0]	Drive Current Level	Swing
0 0	Level 1	400 mV
0 1	Level 2	600 mV
1 0	Level 3	800 mV
1 1	Level 4	1200 mV

Table 6: SMBus Swing Setting of PI3EQXDP1201 Demo Board Rev.A

SMBus Byte 4-7 bit[4:3]	Pre-emphasis Level	Swing
0 0	No Pre-emphasis	0 dB
0 1	Level 1	3.5 dB
1 0	Level 2	6 dB
1 1	Level 3	9 dB

Table 7: SMBus Pre-emphasis Setting of PI3EQXDP1201 Demo Board Rev.A

If setting the swing and pre-emphasis values to the highlighted sets above for all four lanes, 18h will be written to bytes 4-7. Below is an example to set equalization, swing and pre-emphasis via SMBus control.

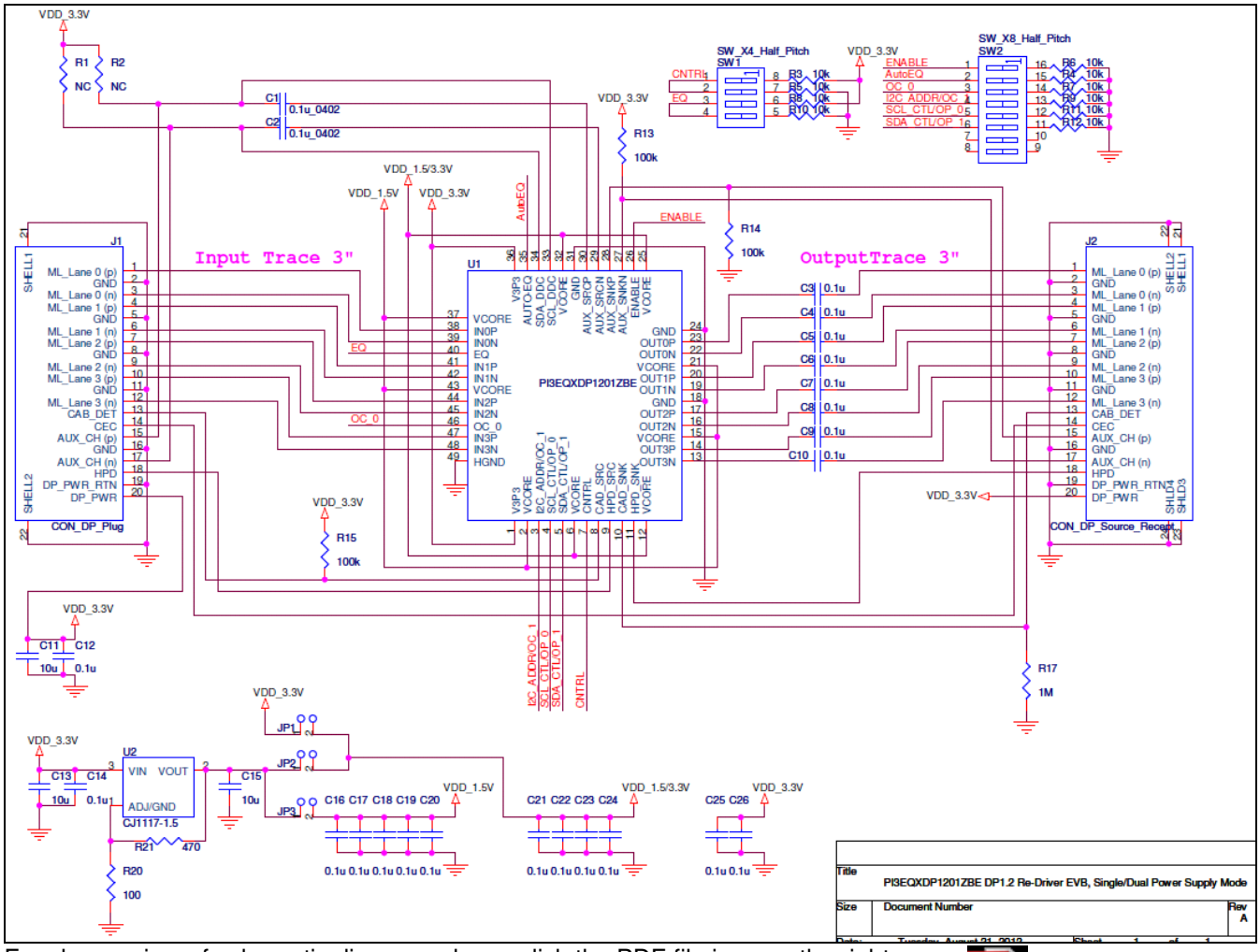
SMBus Address	R/W	Data Bytes
A8 or AA	W	04, 00, 18, 18, 18, 18

Table 8: Swing and Pre-emphasis Settings of PI3EQXDP1201 via SMBus

6 Relative References

(1) VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010
(2) VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012
(3) VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009

7 Appendix A: Demo Board Schematic



For clearer view of schematic diagram, please click the PDF file icon on the right.

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